MULTIMEDIA UNIVERSITY ™

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2, 2022/2023 (TERM:2220)

ERE1136 – DIGITAL DESIGN

(Intelligent Robotics)

JULY 2023
9:00 a.m – 11:00 a.m
(2 hour)

INSTRUCTIONS TO STUDENTS

1. This question paper consists of 5 pages with **4 questions** only.
2. Answer **ALL** questions. All questions carry equal marks and the distribution of the marks for each question is given.
3. Please print all your answers in the Answer Booklet provided.

Question 1

(a) Describe the concept of a signal, then state its relationship with physical quantities. **[4 marks]**

(b) List **three** advantages of a digital system over an analog system. **[3 marks]**

(c) Convert the following decimal number 35_{10} into the following bases. Show the working steps for each conversion.

(i) Base-2 **[2 marks]**
(ii) Base-8 **[2 marks]**

(d) Given three numbers as shown in **Table Q1(d)**, answer the following:

Table Q1(d)

Number 1	Number 2	Number 3
76_{10}	70_8	56_{16}

Convert all the given numbers (Numbers 1, 2 and 3) to binary, Gray code and BCD (binary coded decimal) representations, respectively. Show clearly all the working steps. **[9 marks]**

(e) Perform the following operations in 8-bit two's complement notation for both the operands and result. Comment on the discrepancy, if any.

(i) Add -37 to 95 **[2.5 marks]**
(ii) Subtract 43 from -88 **[2.5 marks]**

Continued.....

Question 2

(a) Simplify the Boolean expression below using **Boolean algebra**. Show each simplification step clearly.

$$ABCD + (\overline{AB})CD + AB(\overline{CD})$$

[5 marks]

(b) Develop a **truth table** for the expression below:

$$\overline{A}B + \overline{A\overline{C}} + AB\overline{C} + A\overline{B}\overline{C}$$

[5 marks]

(c) Find the minimum Sum of Products (SOP) logic expression of output Y using Karnaugh map for the truth table in **Table Q2**.

Table Q2

Inputs				Output
A	B	C	D	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

[5 marks]

(d) Determine the minimum Sum-of-Products (SOP) form with 'don't care' conditions using the Quine-McCluskey method for the following functions. List all possible minimized solutions.

$$f(A,B,C,D) = \Sigma m(1, 2, 4, 8, 10, 14) + d(6, 7, 11)$$

[10 marks]

Continued.....

Question 3

(a) Draw the timing diagram of the clock (CLK) and complete, Q_0 and Q_1 signal of the counter shown in Figure 3 (a) for **6 clock pulses**. Assume the initial condition for all Q is low.

[6 marks]

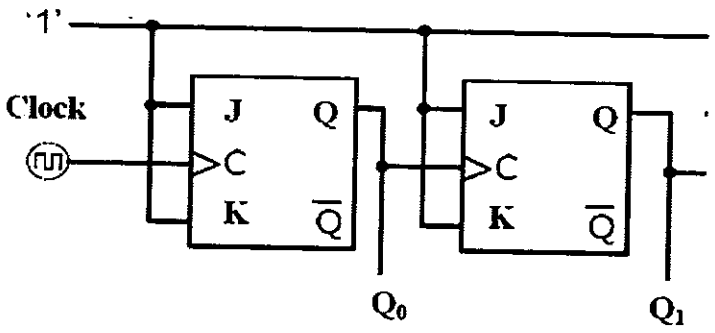
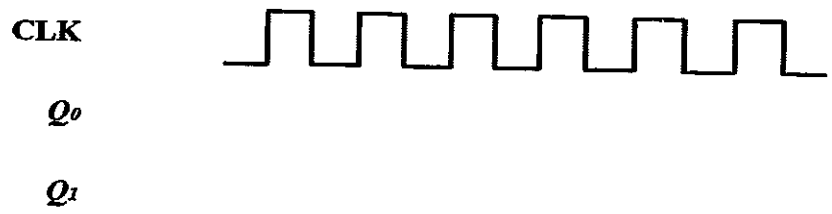


Figure 3 (a)



(b) Using negative edge-triggered T flip-flops, construct the following counters to generate the counting sequence shown in Figure 3(b):

(i) Asynchronous counter (Illustrate the sequential logic circuit of the counter).

[6 marks]

(ii) Synchronous counter (Show all necessary design steps and illustrate the sequential logic circuit of the counter).

[13 marks]

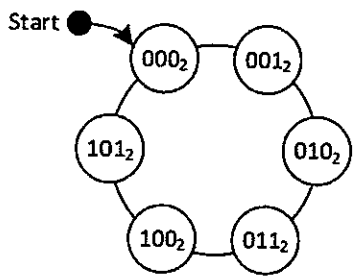


Figure 3(b)

Continued.....

Question 4

(a) Implement the switching function $f(x, y, z) = \sum m(0,1,2,4,6,7)$ for 3-to-8 decoder with active low outputs.

[Hints: Use 2-inputs logic AND gate for active low output.]

[5 marks]

(b) With the aid of a schematic diagram, suggest a way to make one 4-to-16 decoder using multiple 2-to-4 decoders with enable input. Number the inputs and outputs of the decoders. (Note: Draw the entire working diagram clearly).

[10 marks]

(c) Design a logic circuit to realize the function of f with the use of a single 8-to-1 multiplexer with active high output. Show the truth table and the logic circuit diagram.

$$f(b, c, d) = \sum m(0,2,3,5,7)$$

[8 marks]

(d) Draw a schematic symbol of a 1-bit full adder, showing its inputs and outputs.

[2 marks]

End of Paper